

Figure 1

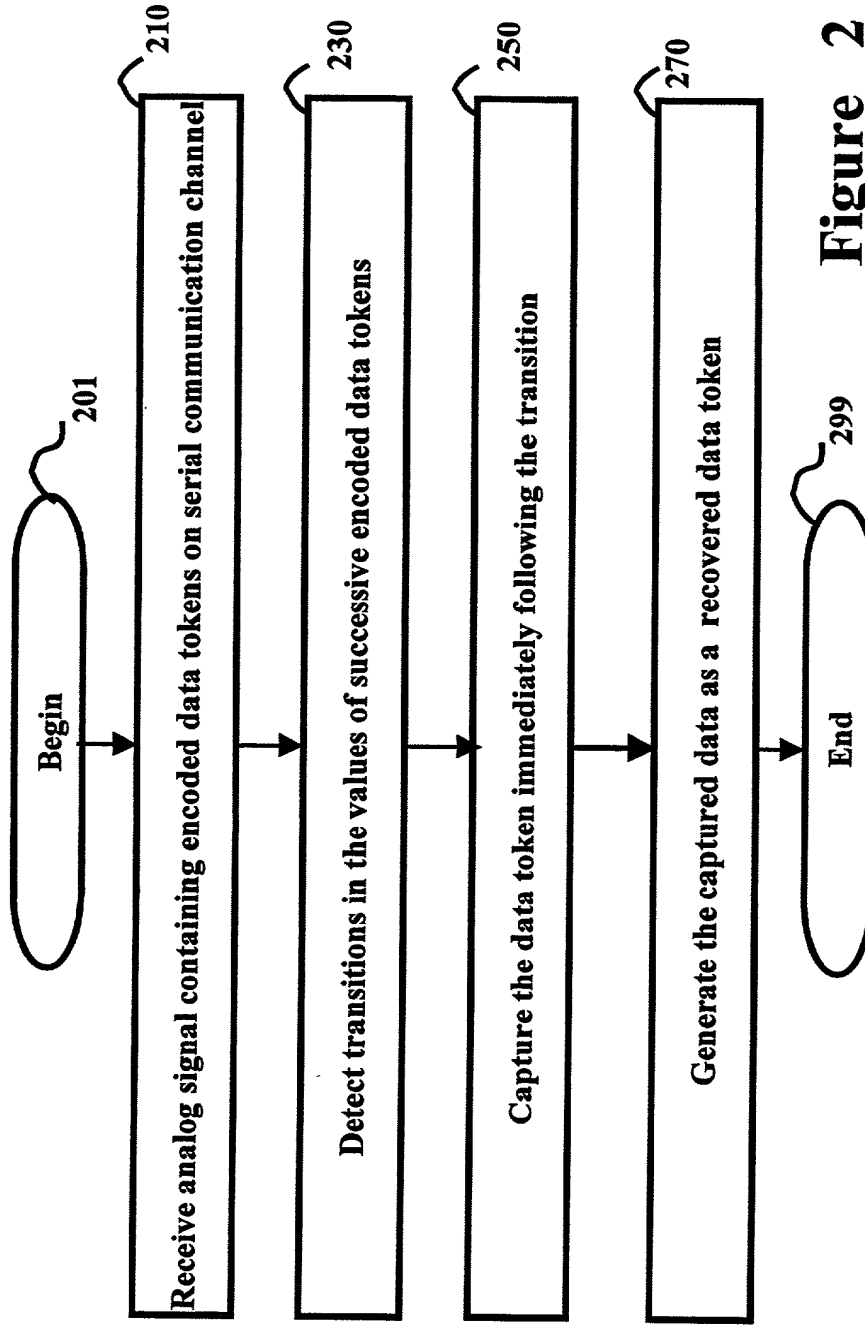


Figure 2

FIGURE 3 is a block diagram of a system for processing a signal. The system includes a clock recovery circuit, a sampler circuit, a delay block, a PTD, a comparator, a flip flop, and a multiplexer. The clock recovery circuit receives a signal from a delay block and outputs a clock signal to the sampler circuit. The sampler circuit receives a signal from a delay block and outputs a signal to a PTD. The PTD outputs a signal to the comparator. The comparator outputs a signal to a flip flop. The flip flop outputs a signal to a multiplexer. The multiplexer outputs a signal to a delay block. The delay block outputs a signal to the clock recovery circuit. The system is shown in a block diagram format with various components and their interconnections.

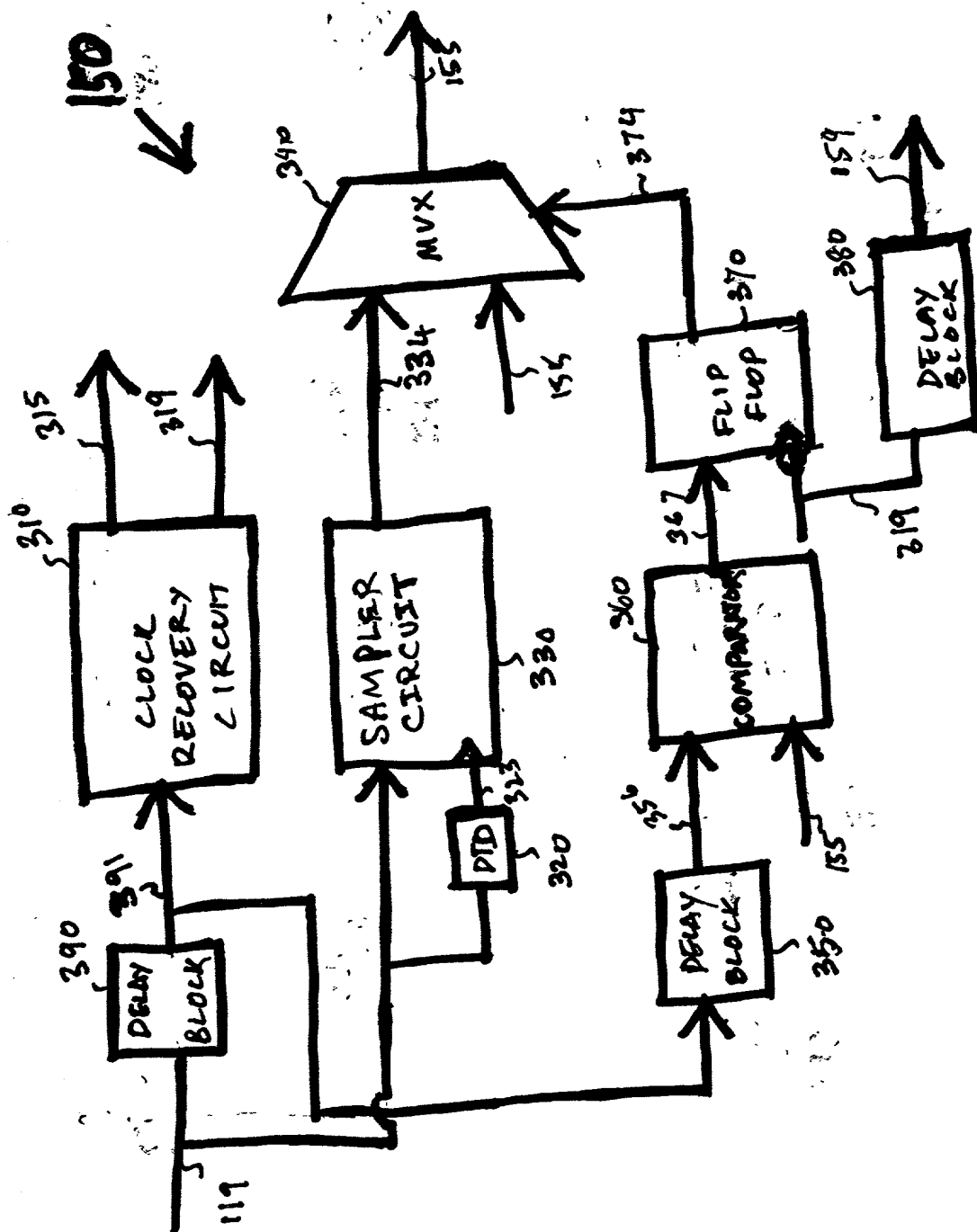


FIGURE 3

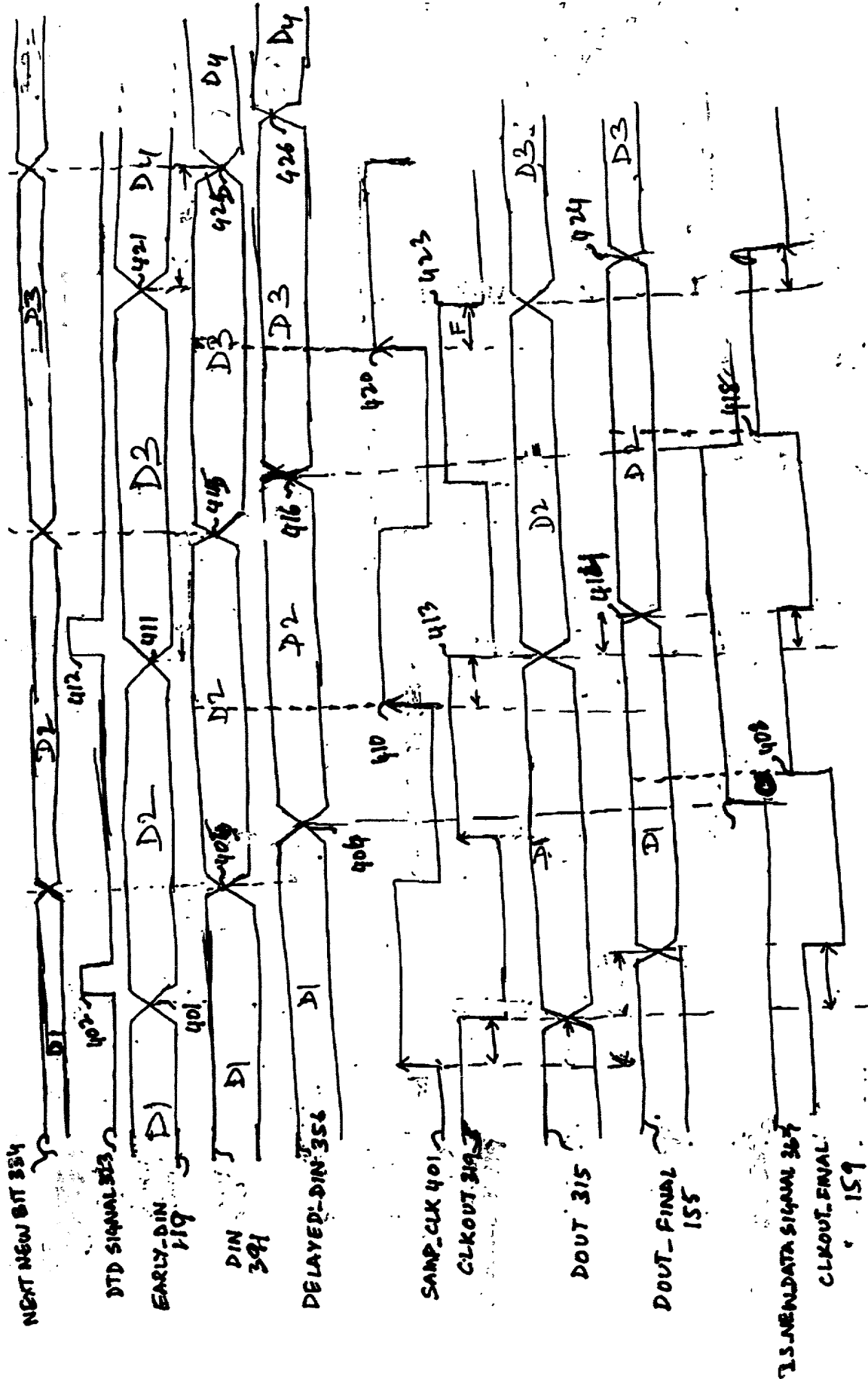


FIGURE 4